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Evaluation of Logic Families using NOR and NAND Logic Gates

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Abstract- ***A logic gate is an idealized or physical device that implements a Boolean function. They are the fundamental building block for high performance data path circuits. Logic gates are implemented using diodes or transistors In this paper different logic circuit families under NAND and NOR logic are analyzed. Their performance in terms of power, speed and power-delay product are of particular interest. CMOS circuit with different scaling has also been compared from 180nm - 22nm.***

Keywords- **CMOS, delay, NAND, NOR, power, power-delay product, scaling.**

I. INTRODUCTION

A logic family of monolithic digital integrated circuit devices is a group of electronic logic gates constructed using one of several different designs, and with compatible logic levels and power supply characteristics within a family. Many logic families has been produced as individual components, with each containing one or few related basic logical functions, which could be used as "building-blocks" to create systems to interconnect more complex integrated circuits. A "logic family" may also refer to a set of techniques used to implement logic within VLSI integrated circuits such as central processors, memories, or other complex functions. In the present work, NOR and NAND gate is evaluated using RTL, DTL, TTL, ECL and CMOS structures. CMOS logic has also been evaluated for different scaling in NOR and NAND gate.

II. LOGIC FAMILIES

A. RTL

RTL stands for Resistor Transistor Logic. In this logic, transistor is used in conjunction with resistors to create a logic circuit. The NPN transistors that are used in RTL logic acts as an inverter circuit. When high (Logic '1') input is applied at gate, then transistor turns 'ON' and low (logic 0') is obtained at the output.

An RTL NOR gate circuit consists of two transistors Q1 and Q2 connected as shown in fig 1. When either of input In1 or In2 is driven to high value, corresponding transistor goes to the saturation and output is pulled to low value. When both the inputs In1 and In2 are driven to low value, corresponding transistor goes to OFF state and output is pulled to the high value.

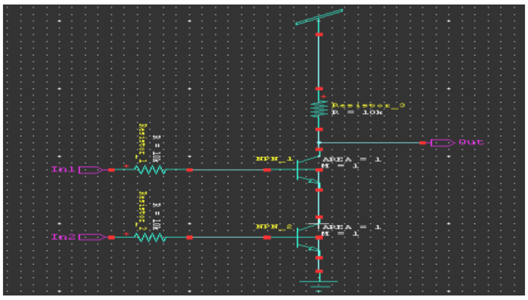

Fig. 1 RTL NOR gate

B. DTL

DTL stands for Diode Transistor Logic. In this DTL, the logic function is implemented by using diodes and transistors. Each of the input is associated with one diode. Figure 2 shows DTL NOR logic circuit. Here diode acts as 'OR' circuit and is connected to a transistor inverter that acts as a 'NOT' circuit. As inputs going high value, the corresponding diode conducts current, through the resistor. This turns 'ON' the transistor. Thus transistor act as short circuit and is grounded. At the output, low value is obtained. If input In1 and In2 are Low, the diodes do not conduct and thus output is at High value.

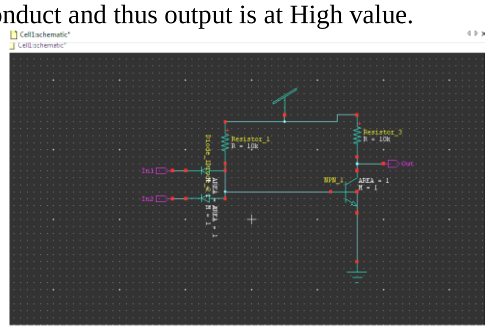

Fig. 2 DTL NOR gate

C. TTL

TTL stands for Transistor-Transistor Logic. Figure 3 shows TTL NAND gate.

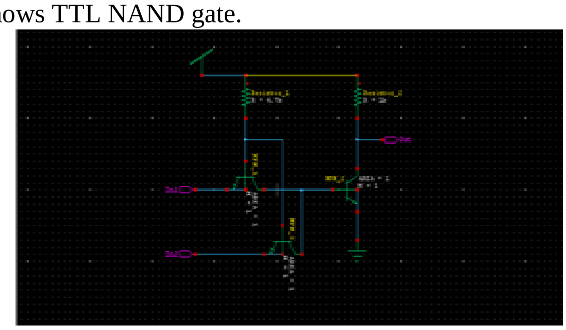

Fig. 3 TTL NAND gate

When both inputs In1 and In2 are high, the two transistors which are on the left are in reverse active state.

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The current flows through the resistor through base and collector of these transistors, and then through the base of transistor on the right, saturating it and bringing the output down to ground value. When both of the inputs In1 and In2 are low, then the easiest path to ground through the resistor is through the base of the transistors on the left to the inputs. This brings their collector voltages to low value so that very little current can flow through the base of the transistor on the right. Thus it keeps that transistor off, bringing the output to the high value. When only one of the inputs were low, that input provides the easiest path to the ground, through its corresponding transistor. This keeps the transistor on the right switched off.

D. ECL

ECL stands for Emitter Coupled Logic. ECL is the fastest non-saturating form of digital bipolar circuits. In non-saturating architecture transistor stores less charge in their bases and thus switches much faster than the saturating circuit architectures such as TTL. Figure 4 shows the ECL NOR gate structure.

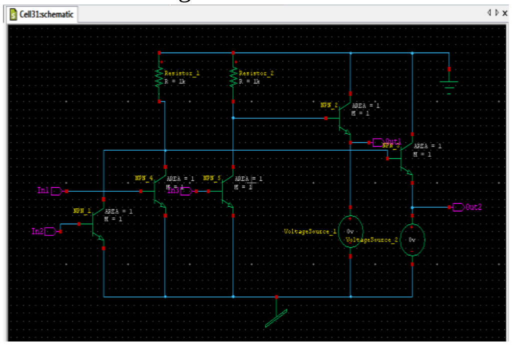

Fig. 4 ECL NOR gate

When both the inputs In1 and In2 are Low, then Q3 becomes more forward biased keeping itself ON and thus Q1 and Q2 remains OFF. Therefore output 'Out' is high. When In1 or In2 or both are high, then corresponding transistor turns ON, keeping Q3 OFF. Thus the output 'Out' is Low.

E. CMOS

CMOS stands for Complementary Metal Oxide Semiconductor. It uses complementary arrangements of N-channel and P-channel Field Effect Transistor. The initial devices used oxide-isolated metal gates, so they are called CMOS. CMOS NOR gate is shown in figure 5.

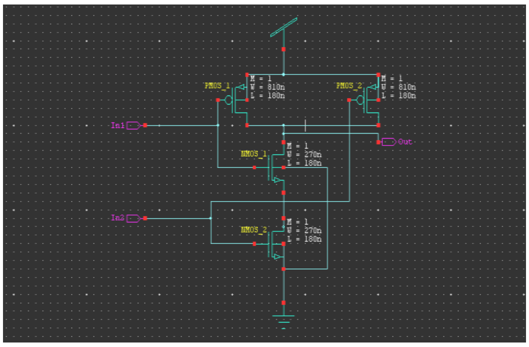

Fig. 5 CMOS NOR gate

Scaling

Scaling of power supply voltage is one of the major factors for reduction in the power consumption. Threshold voltage may be reduced to get higher drive current and thus better speed, but this increase in the stand-by power. The technique to achieve low power is to operate the circuit with supply voltage lower than the threshold voltage that is sub threshold region.

CMOS circuits at different scaling

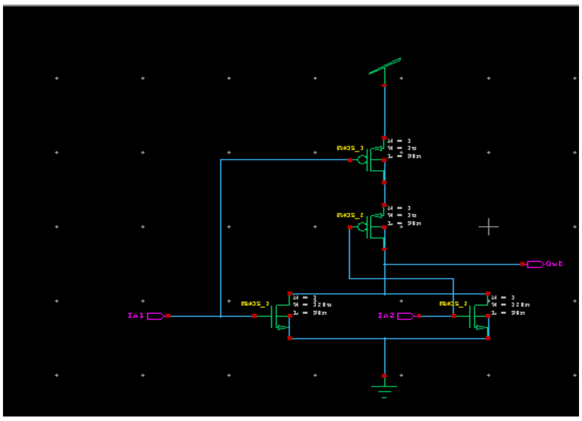

Fig. 6 CMOS circuit with 180nm scaling

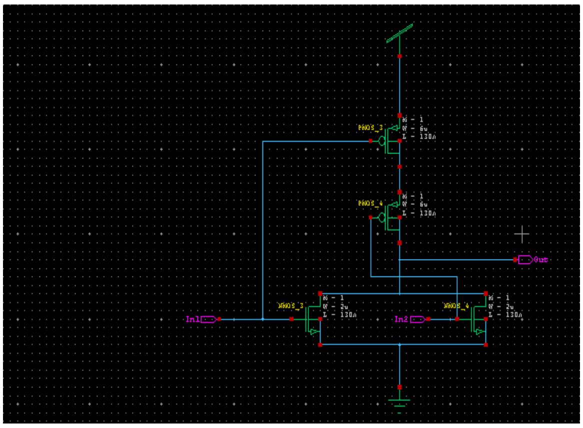

Fig. 7 CMOS circuit with 130nm scaling

III. RESULTS & DISSCUSSION

The output waveforms are shown in figure 8 and figure 9. The x axis shows the voltage level in volts and y axis shows time in seconds. The input voltage level is given by V(In1) and V(In2). The corresponding NAND logic output and NOR logic output can be observed from the V(out). It can be seen that if both of the two inputs are at high logic level, the corresponding output shows logic '0' and if both the inputs are low, then output is at logic '1' for NAND logic. Simulations has been performed for the RTL, DTL, TTL and CMOS family for NAND logic and NOR logic. The output waveform shown in fig 8 is of CMOS NAND logic and in fig 9 is CMOS NOR logic.

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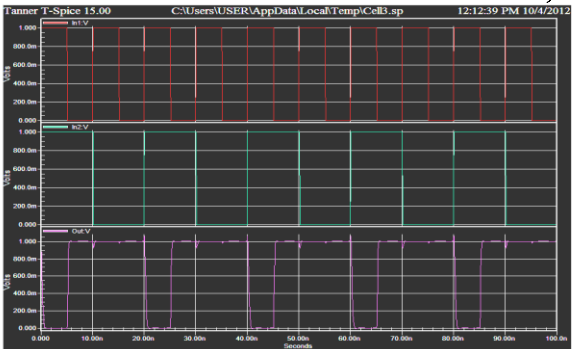

Fig. 8 Output Waveforms (NAND)

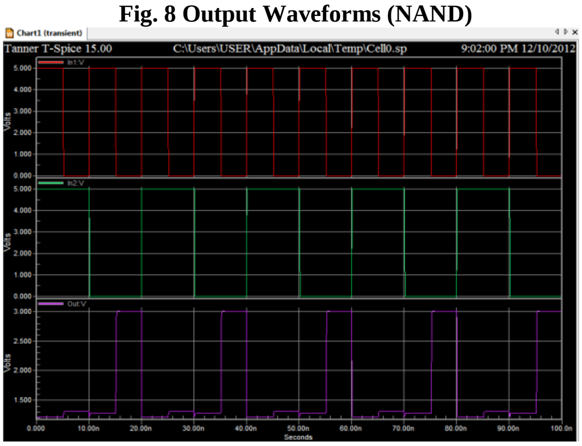

Fig. 9 Output Waveforms (NOR)

Table 1 shows the comparison between RTL, DTL, TTL and CMOS logic families under the NOR and NAND logic. The simulation had been carried out at power supply voltage value of 3 V. Power, delay, and power-delay products are some of the performance parameters considered for comparison between various logic families.

Table 1 Comparison of different Logic families under NOR and NAND Logic

	NOR Gate			NAND Gate		
Logic Families	Power	Delay	Power-Delay product	Power	Delay	Power-Delay product
RTL	6.69 E-03	2.49 E-11	1.67E -13	4.43 E-04	3.11E+ 01	1.38E -02
DTL	3.96 E-03	6.01 E-11	2.38E -13	9.59 E-04	7.69E+ 01	7.37E -02
TTL	1.56 E-02	3.05 E-11	4.76E -13	3.59 E-03	3.06E+ 01	1.10E -01
CMOS	4.62 E-04	5.54 E-11	2.56E -14	4.62 E-06	6.91E+ 01	3.19E -04

Table 2 shows the comparison of CMOS logic families for different scalings in NOR and NAND logic.

Table 2 Comparison of CMOS logic families for different scaling.

	NOR Gate			NAND Gate		
Length	Power	Delay	Power-Delay product	Power	Delay	Power-Delay product
180nm	9.61E-04	5.54E-11	5.32E-14	4.62E-06	6.91E-11	3.19E-16
130nm	8.89E-04	1.60E-11	1.42E-14	1.65E-06	5.96E-11	9.81E-17
90nm	7.55E-04	1.12E-11	8.45E-15	7.91E-07	4.66E-11	3.69E-17
65nm	6.59E-04	3.01E-12	1.98E-15	5.31E-07	3.88E-11	2.06E-17
45nm	5.47E-04	-1.47E-11	-8.06E-15	3.48E-07	3.39E-11	1.18E-17
22nm	3.99E-04	2.03E-11	8.11E-15	3.06E-07	3.24E-11	9.90E-18

IV. CONCLUSION

This paper provides comparison of different logic families in terms of power, delay and power-delay product. The circuits are evaluated for both the NAND and NOR logic. It has been observed that the power consumption and power-delay product of CMOS logic families are at the minimum. Thus CMOS families outperforms in performance parameters as compared to other logic families. Scaling of circuit for different length has also been observed and tabulated.

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